Patent
Attorney's Docket No. 030682-103

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

#7
9/5/03

In re Patent Application of	)	
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Hiroyuki KAWAI et al.	)	Group Art Unit: 2124
	)	
Application No.: 09/667,783	)	Examiner: C. Ngo
	)	
Filed: September 22, 2000	)	Confirmation No.: 1075
	)	
For: SQUARE ROOT EXTRACTION CIRCUIT AND FLOATING-POINT SQUARE ROOT EXTRACTION DEVICE	)	

REQUEST FOR RECONSIDERATION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants respectfully request reconsideration of the above-captioned application. The Office Action of June 30, 2003 includes a rejection of the sole claim in this divisional application under 35 U.S.C. §102(b) as allegedly being clearly anticipated by the DeTroye patent (U.S. Patent 4,748,581). Applicants respectfully traverse this rejection.

The DeTroye patent is of the type of conventional square root extraction circuit described at pages 1 and 2 of the present application insofar as it uses CAS (Controllable Add/Subtract) cells which have complicated internal structures, as shown in Figure 1. As described at column 1, lines 10-15, of the DeTroye patent points out that CAS cells have an input for a control signal p. When the control signal p is a logical "0", the CAS cell operates as a full adder circuit and, when the p is "1", the CAS circuit operates as a subtract circuit.

At first blush, the DeTroye patent is confusing because it includes statements such as "all circuit BOA 11, 21, 22, 32, 33, 43, 44, 54, ...receive a binary signal having...the logic value "0" (zero) on their control input (for the signal p)." However, a detailed and careful reading of the patent indicates that the other CAS circuits BOA 12, 13, 33 14, 24 and 34 do not receive only a binary 1, but instead are "controlled by the last bit q_k formed (of the root to be determined) from the preceding sub-circuit k, as explained at column 3 lines 19-27. This is reiterated in claim 1 of the DeTroye patent in the second to the last sub-paragraph at column 4, lines 36-41.

Hence, the DeTroye patent is unlike the present invention insofar as the present invention uses an algorithm that allows for the formation of a square root extraction circuit which comprises only existing adders (full adders FA and half adders HA) as illustrated in the exemplary embodiment of Figure 2 without using controllable add/subtract circuits as has been used in the DeTroye patent.

Stated in terms of the claim language, claim 1 expressly recites that the square root extraction algorithm includes an algorithm:

> "for determining the square root data on the basis of said input data by only additions of square root partial data q(1) to q(m) in q(1) to q(m) order, said square root extraction circuit comprising:
>
> first to *m*th digit calculating portions each including a plurality of adders connected in series so that carries are propagated therethrough, wherein respective ones of said adders which are connected in the last position in said first to *m*th digit calculating portions provide carry outputs serving as said square root partial data q(1) to q(m), respectively, in accordance with said square root extraction algorithm. (Emphasis added)

Hence, Applicants respectfully submit that the DeTroye patent does not anticipate any of the claims of the present application. Further, it does not appear that there would be any motivation found in the prior art to abandon the basic approach articulated in the DeTroye patent that would result in the present invention as articulated in claim 1 without the assistance of Applicants' own teachings.

In light of the foregoing, Applicants respectfully request reconsideration and allowance of the above-captioned application.

Respectfully submitted,
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